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DESIGN OF CMOS HIGH FREQUENCY RING OSCILLATOR WITH 4 VOLTS SUPPLY VOLTAGE

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Abstract:
The performance analysis and characterization of the CMOS High Frequency Voltage Controlled Ring Oscillator are the main motive of this article (HFVCRO). The performance analysis for various HFVCRO techniques at various supply voltages is based on high frequency, low area. Higher frequency is shown in the results, which can be suited for applications across a variety of domains. Another benefit is that the frequency of the HFVCRO is growing quickly as the supply voltage is reduced. This paper offers designers guidance in selecting the best voltage control ring oscillator (HFVSRO) for a given set of applications.
Keywords: CMOS, Inverter, Ring Oscillator, High Frequency, Reverse Voltage

1. Introduction

An oscillator is a circuit that produces output without input. It produces sinusoidal and nonsinusoidal waveforms. An oscillator is called as opposite of the rectifiers, as they convert dc energy to ac while rectifiers convert ac to dc. The oscillator circuit consists of a tank circuit, amplifier, and feedback circuit. A voltage-controlled ring oscillator is one of the basic building blocks of analog and digital circuits.[1]-[6]. Many different implementations of VCOs (Voltage Controlled Oscillator) are there. One of them is the ring oscillator that is commonly used in the clock generation subsystems. Because of its easy integration, the ring VCO is popular. In many digital and communication systems, ring oscillators have become an essential building block due to their integrated nature.

The voltage-controlled oscillator is an electronic device that plays an important role in communication systems due to its high-frequency capability, low power consumption, and

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wide frequency range of operation. To generate a repeated voltage waveform at a particular frequency, it uses feedback, amplification, and a resonant circuit[7]. With an applied voltage, the frequency is varied. VCOs are an important part of the Phase-Locked Loops, Frequency Synthesizers, and almost all digital and analog systems.

An oscillator is a circuit that acts as an amplifier and produces its input waveform. The purpose is to generate a waveform which is constant in amplitude and frequency. The most basic CMOS oscillator uses N odd number of single-ended inverters connected in a chain. The output of the Nth stage is fed-back to the first stage input. No stable operation point exists,Because of the odd number of inversions. Barkhausean criteria must be satisfied to sustain Oscillations. Also, Every stage should add a 180/N phase.

The Block diagram of N stage ring VCO is as shown in the figure:

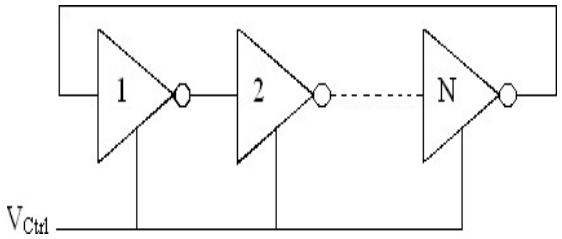

Fig 1 : N Stage Ring VCO

Barkhausen Criteria:

To operate the circuit as an oscillator, The Conditions which are required are called as "Barkhausen criterion". This criterion was first introduced by a german physicist named Heinrich Georg Barkhausen in 1921[8]. To ensure the sustained oscillations, The Barkhausen criteria should satisfy by an amplifier with positive feedback. To maintain the oscillations, the feedback signal itself should be sufficient since there is no input signal for an oscillation circuit.[9]. The Barkhausen criterion states that:

- The gain loop is equal to unity, i.e, $|\beta A| = 1$ and The product βA is called as the "loop gain".
- The phase shift of the loop is zero or 180°.

The requirements of VCO for different applications include high frequency, phase stability, low power consumption, low cost, less area, linearity of frequency on the control voltage, and high gain factor. The Design of Ring VCO involves tradeoffs in terms of speed, area, power, and frequency [10]. The theme of this paper is to design the current starved ring VCO. The rest of the paper includes the literature survey, followed by the proposed system. Further, the results and analysis of the current starved ring VCO and the conclusion is discussed.

2. Related Work

The oscillators are the circuit that produces clock signals. These are required for on-chip applications. The on-chip applications are the biometric sensors and SOCs. A relaxation

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oscillator is implemented as part of the sensor to provide the clock reference. A clock reference is not desired on the outside of the sensor because of its limited applications [11]. The oscillator has a balanced accuracy performance with a low-cost advantage due to an RC implementation. To provide the clock inside the sensor an RC relaxation oscillator is chosen. To achieve low-frequency standard deviation across different supplies, temperatures, and process corners a current mode relaxation oscillator is proposed. A 1.8V nominal voltage and a 0.18 µm technology are used. The output frequency of 78.3 MHz frequency can be obtained. Also, compare the relaxation oscillator and the proposed design. The construction of a high-speed clock for data communication is made by the high-frequency variable oscillator [12]. To use in data communication for reliable and fast data transmission a wide variable frequency oscillation is designed. In the design, we use a voltage-controlled oscillator in a Colpitts configuration. For a reverse-biased voltage (VR) of 0 to 25V, the design is capable of producing an 800 MHz frequency while maintaining a good tuning flatness throughout the range.

3. Design of Voltage Controlled Oscillator

In methodology, the current starved ring VCO had introduced. Delay should be voltage controlled, as the frequency of oscillations depends on the delay produced by each inverter stage. The delay can be controlled by controlling the amount of current available to charge or discharge the capacitor load [13]. We call this type of circuit current starved ring VCO. In this VCO, the control voltage will turn on resistances of pull-up and pull-down transistors through a current mirror. These resistances can control the current available to the capacitor load. When the control voltage is large, a large current will flow and produces a small resistance, which results in a small delay.

The current starved ring VCO diagram is shown with PMOS NMOS And inverter below figure:

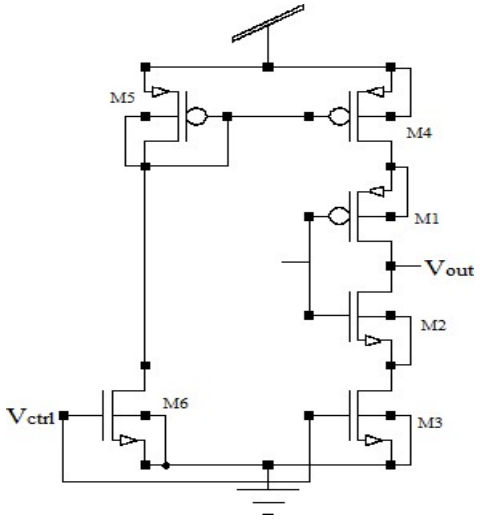

Fig 2 : Proposed Current Starved Ring VCO

From figure, the transistors M5 and M8 operate as an inverter that is connected in series and

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while M1 and M11 act as current sources. This will bind the availability of currents to the M5 and M8 transistors the currents are the same for each inverter. Control voltage via current mirror is used to modulate the resistances of the pull-up and pull- down transistors [14]. By using variable resistances, the controlling of current to charge or discharge the load capacitances is done. The large value of control voltage permits a huge current to flow, responsible for small resistance, less delay, and high frequency. This type of VCO employs variable bias current to ensure complete command of the frequency of oscillation, which leads to the high oscillation frequency.

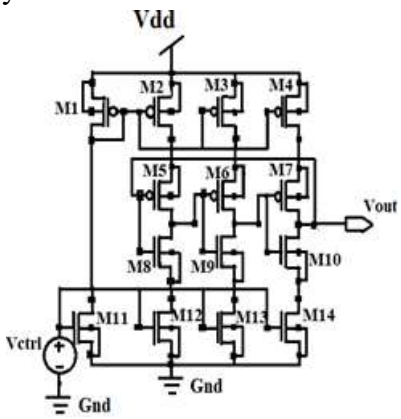

Fig. 3 : Schematic diagram of three stage current starved ring VCO

With the support of small signal corresponding ideal of single delay cell of current starved ring VCO, the final gain of single stage CS ring VCO can be expressed as

$$\frac{\Delta V_{out}}{\Delta V_{in}} = 2$$

The frequency of oscillations F_{OSC} for current starved ring oscillator can be expressed in accordance with the total capacitance (C_{total}), input control voltage (V_{ctr}), current (I_d) and count of delay stages (N)

$$f_{osc} = Id/2*N*C_{total}*V_{cts}$$

Where C_{total} = Total capacitance, V_{ctr} = Input control voltage, Id = Current, N= count of delay stages. The considered VCO over a temperature range from - 40^0c to 125^0c it is producing a frequency of 1.06GHz& the elongation is accomplished above a kind of frequency as of 970MHz to 1.03GHz.

4. Results and Analysis

The schematic diagram for 3 stage ring VCO is shown below:

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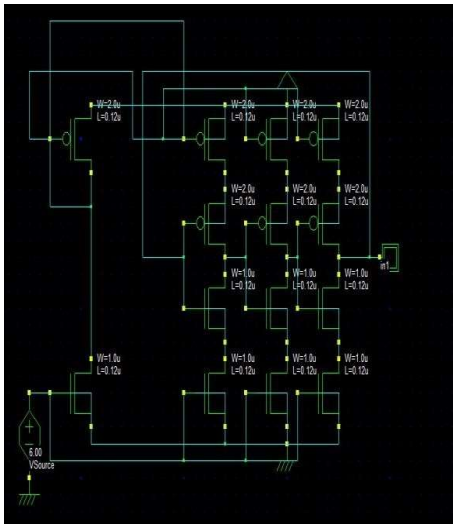

Fig 4 : Schematic diagram of three stage current starved ring VCO

The layout of the three stage current starved ring VCO is shown below:

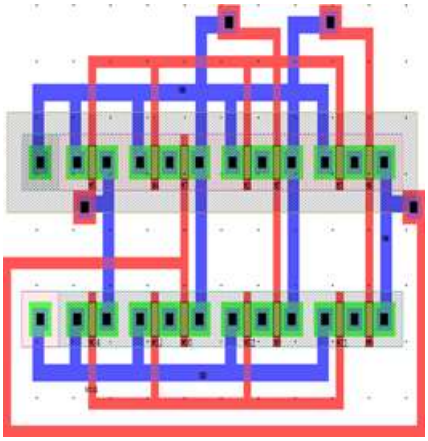

Fig 5 : Layout of three stage current starved ring VCO

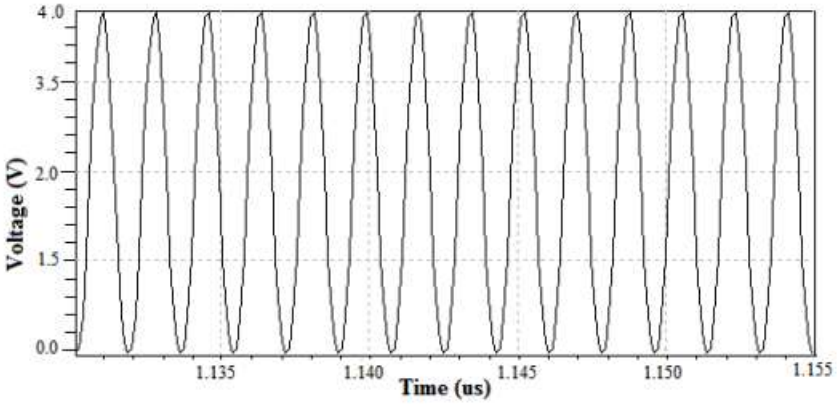

Fig 6 : Output Waveform of the three stage VCO

The following figure represents the frequency versus time graph with control voltage 1V

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CONTROL VOLTAGE (V)	FREQUENCY (GHz)
4.0	1.2
3.0	1.05
2.0	0.8
1.0	0.12

Table 1 : Simulation results of three stage current starved ring VCO at different control voltage

As the above table represents the frequency Versus voltage. We can observe that as control voltage increases the frequency also increases.

5. Conclusion

In this paper the design of current starved ring oscillator is done. The main aspect of this paper is to decrease the delay, therefore the frequency has increased. The results shown here has the frequency of 1.2 GHz. The frequency has been changed as the control voltage changes.

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